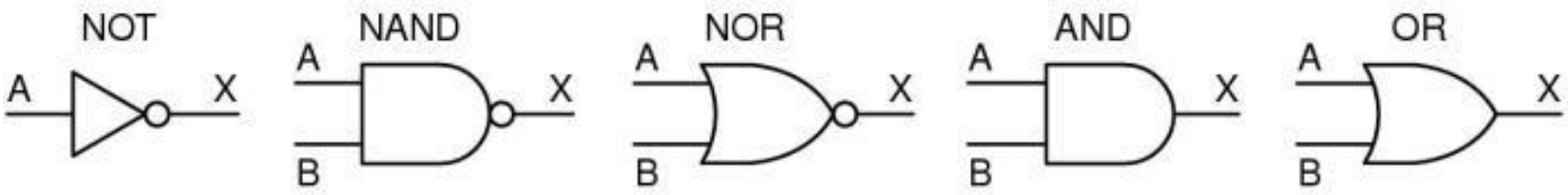
UNIVERSIDADE DO ESTADO DE MINAS GERAIS

Docente: Rildo Afonso de Almeida

Laboratório de Circuitos Lógicos

UEMG

PORTAS LÓGICAS



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(a)

A	B	X
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1	1	0

(b)

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0	1	0
1	0	0
1	1	0

(c)

A	B	X
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0	1	0
1	0	0
1	1	1

(d)

A	B	X
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1	1	1

(e)

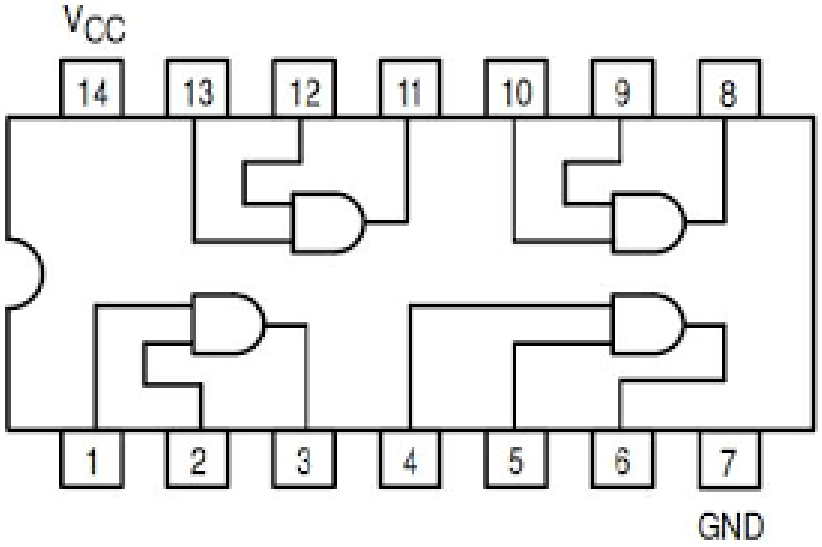
UEMG

PORTAS LÓGICAS

AND

PORTAS LÓGICAS

AND



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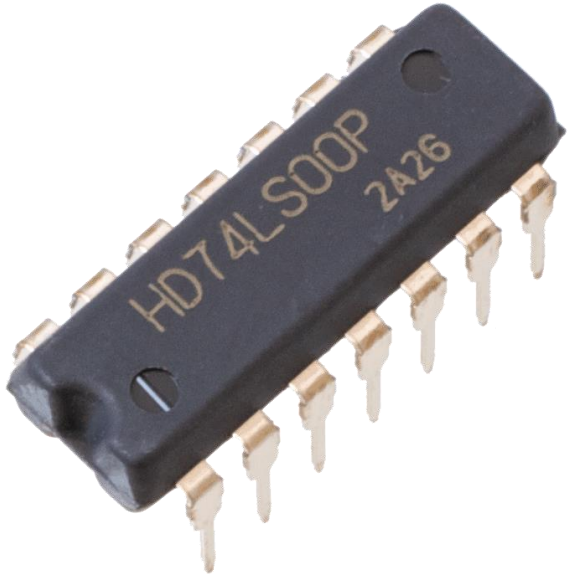
UEMG

PORTAS LÓGICAS

NAND



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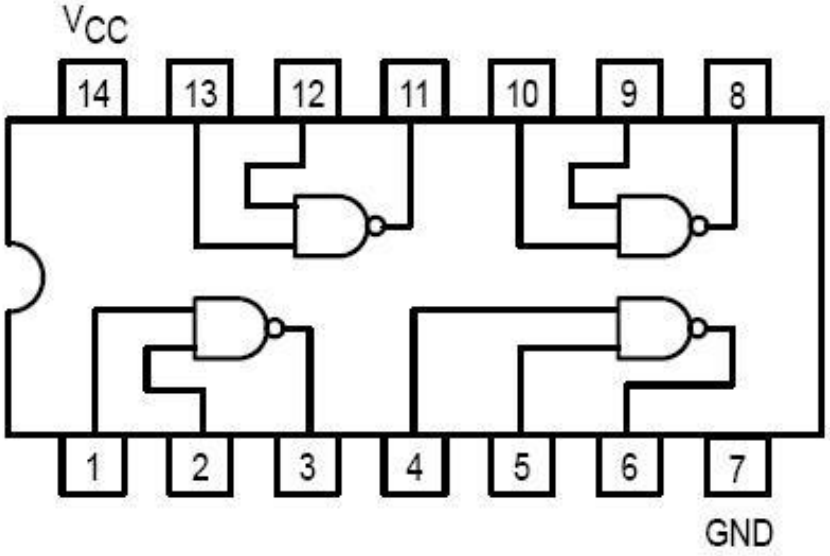
PORTAS LÓGICAS

NAND



A	B	X
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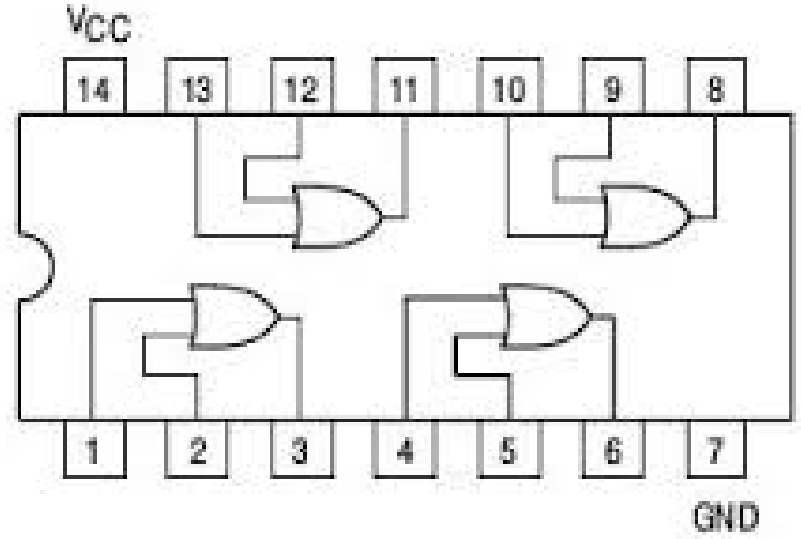
UEMG

PORTAS LÓGICAS

OR

PORTAS LÓGICAS

OR



A	B	X
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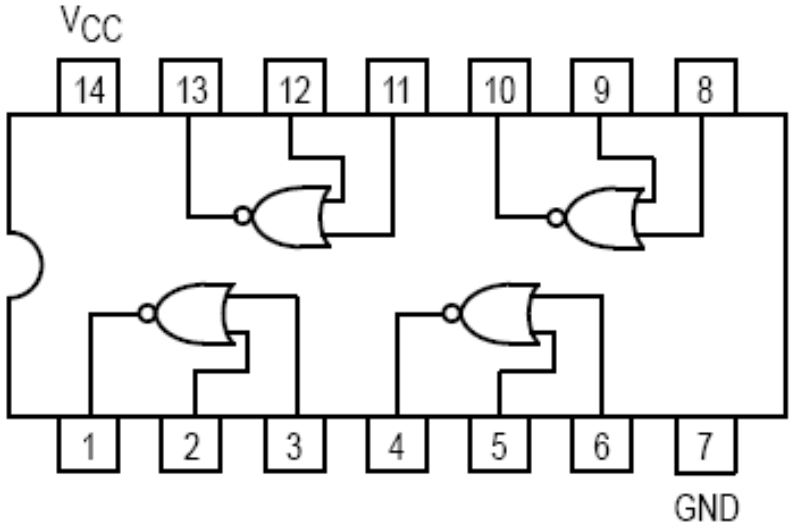
PORTAS LÓGICAS

NOR

PORTAS LÓGICAS

NOR



A	B	X
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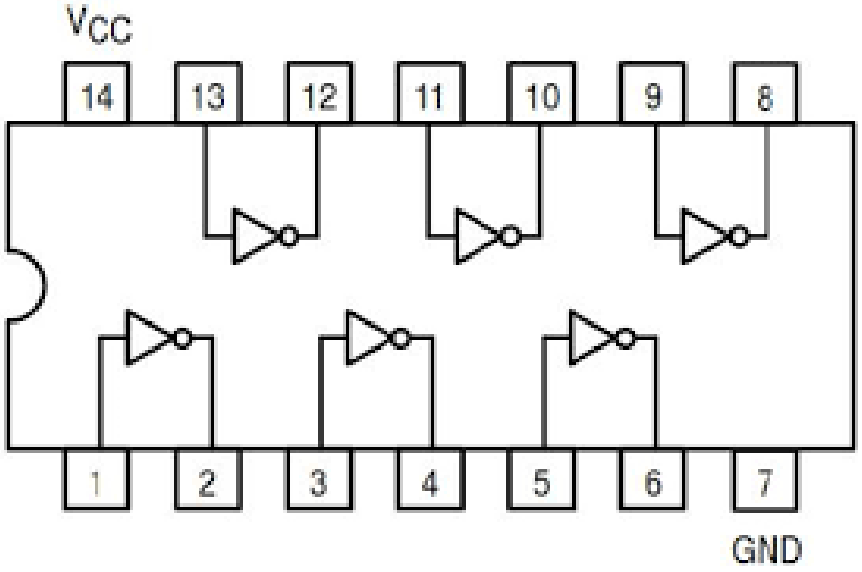
PORTAS LÓGICAS

NOT

PORTAS LÓGICAS

NOT



A	X
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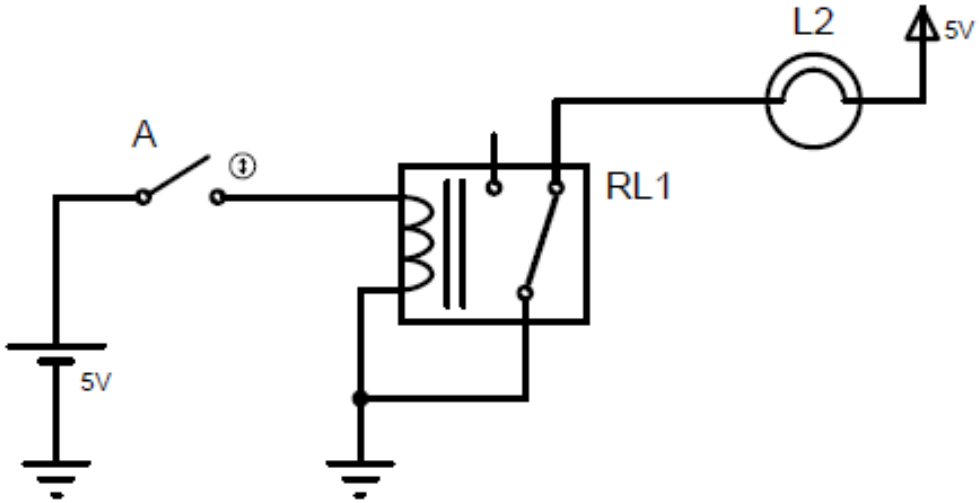
UEMG

PORTAS LÓGICAS

Analogias de Portas Lógicas

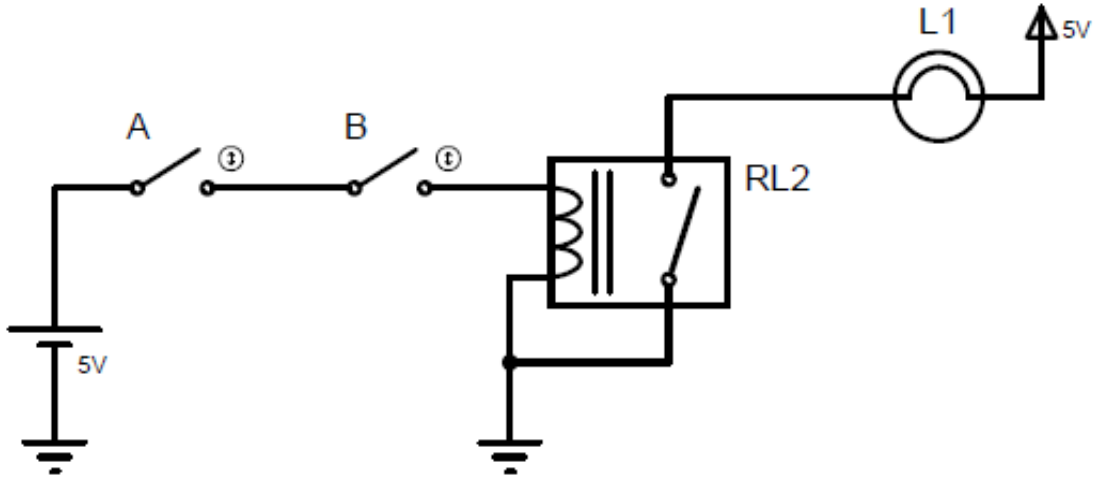
PORTAS LÓGICAS

Lógica NOT - NÃO



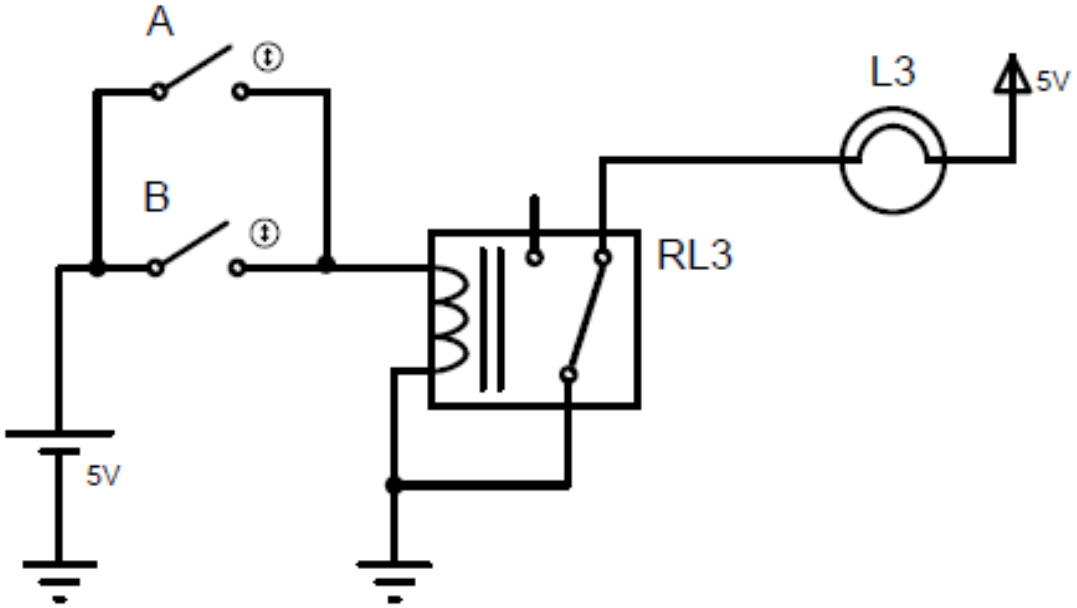
PORTAS LÓGICAS

Lógica AND - E



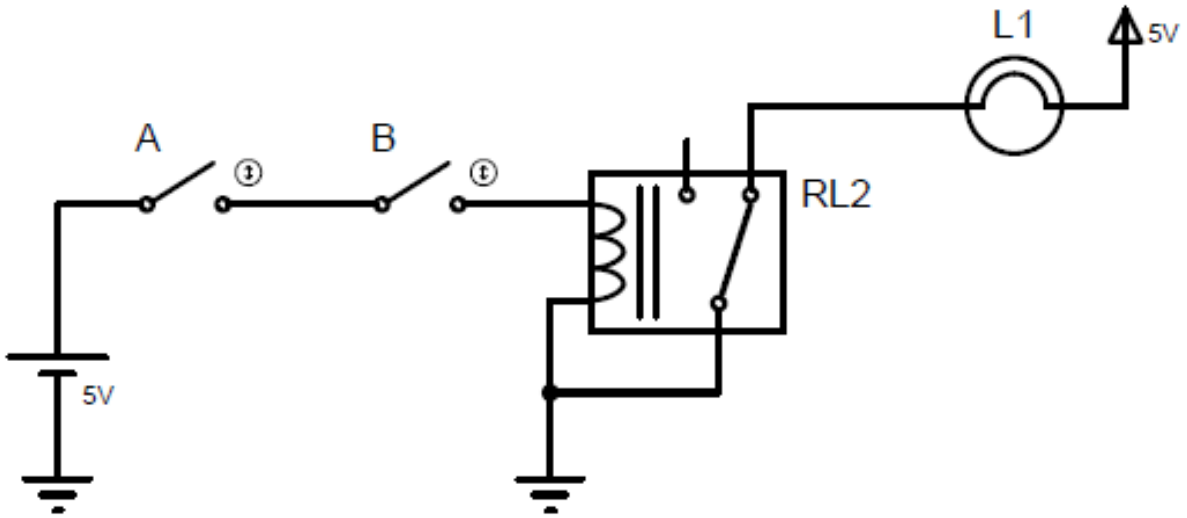
PORTAS LÓGICAS

Lógica NOR - NÃO OU



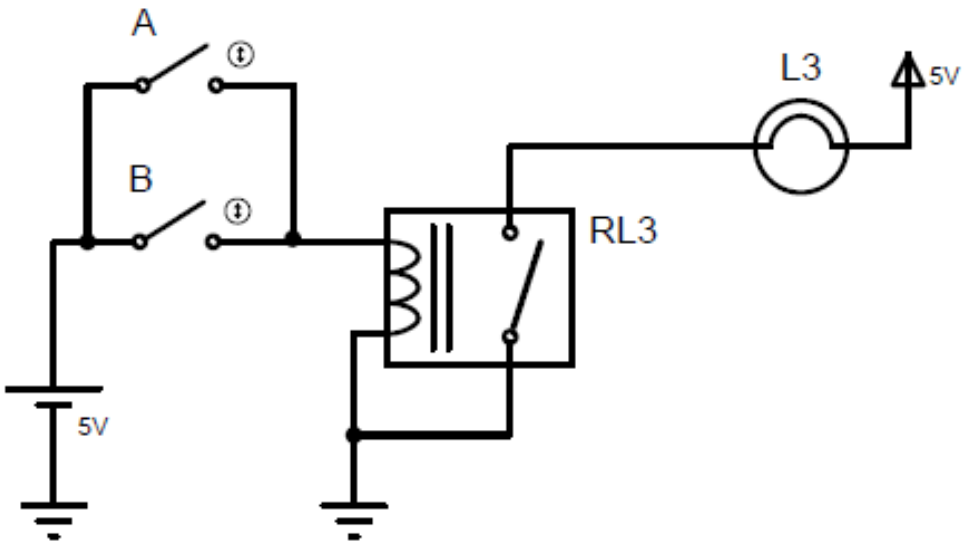
PORTAS LÓGICAS

Lógica NAND - NÃO E



PORTAS LÓGICAS

Lógica OR - OU



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